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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	)	Art Unit: 2186
	)	
Howard S. David	)	Examiner: Dare, Ryan A.
	)	
Serial No: 10/713,486	)	
	)	
Filed: November 14, 2003	)	
	)	
For: PARTIAL BANK DRAM REFRESH	)	

DECLARATION OF HOWARD S. DAVID UNDER 37 CFR 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Howard S. David, declare and state as follows:

1. I am the sole inventor in the above-referenced patent application. Pillsbury Winthrop LLP filed the application on November 14, 2003.

2. On October 23, 2003, I received, in the United States, a draft of the application for my review. I received the draft as an enclosure to a letter and as an attachment to an email (on October 23, 2003) from Stuart B. Chinn, the attorney who drafted the application. Attached as "Exhibit A" is a true and accurate copy of the letter, the email, and the draft of the application.

3. The draft of the application, i.e., the specification and the drawings, show my conception, in the United States, of the invention claimed in U.S. Patent Application Serial No. 10/713,486. The draft application is substantially identical to the application as filed.

4. I have reviewed the Brucke reference, US PG Pub 2005/0088894 cited in an Office

Action dated August 23, 2006. The Examiner stated that the Brucke reference teaches that "multiple rows per memory bank array are refreshed in a staggered fashion per the auto-refresh command". The Brucke reference was filed on October 23, 2003.

5. The application was constructively reduced to practice by the filing of the application in the U.S. Patent Office on November 14, 2003. Thus, the date of invention is at least as early as October 23, 2003.

6. Dependent claims 5, 12, 21, 26, 33, and 40 of the application as filed recite "wherein multiple rows per memory bank array are refreshed in a staggered fashion per the auto-refresh command".

7. Dependent claims 5, 12, 21, 26, 33, and 40 of the draft application (copy enclosed) recite "wherein multiple rows per memory bank array are refreshed in a staggered fashion per the auto-refresh command".

8. Support for the limitation "multiple rows per memory bank array are refreshed in a staggered fashion per the auto-refresh command" can be found in the draft application in various places, including the following:

"Within each bank, it is also desirable to refresh multiple rows, either simultaneously or in a staggered fashion." (Lines 14-15, page 9).

"If refreshing a row takes approximately t_{RC} = 60 ns, and the row refreshes are staggered by about 4 ns, then a 1 Gb DDR2 refresh command would take 60 + 15 * 4 = 120 ns, roughly consistent with the DDR2 specification of 127.5 ns. Using the all bank refresh requires 8192 refresh commands per t_{REF} = 64 ms. Note that the rows are refreshed in a staggered fashion per refresh command to prevent the large current spike that would occur if all rows were refreshed at exactly the same time." (Lines 4-10, page 14).

"FIG. 5 illustrates that during the time t_{RFC} = 127.5 ns, 2 rows per bank, row a and row b, for banks 0-7 are refreshed in a staggered fashion." (Lines 17-18, page 19).

"FIG. 7 illustrates that during the time t_{RFC} = 127.5 ns, 4 rows per bank, rows a, b, c, and

d for banks 0-3 are refreshed in a staggered fashion." (Lines 14-15, page 19).

9. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true, and, further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application and any patent issued thereon.

Howard S. David — 10-17-2007

Howard S. David — Date

Encls: October 23, 2003 letter, email, and draft application.

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~~(8/13/03)~~ APPLICATION FOR
UNITED STATES PATENT
IN THE NAME OF

HOWARD S. DAVID

FOR

PARTIAL BANK DRAM REFRESH

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TITLE OF THE INVENTION

PARTIAL BANK DRAM REFRESH

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to dynamic random access memory (DRAM), and in particular to refreshing techniques.

2. Discussion of the Related Art

Memory devices are widely used in many electronic products and computers to store data. A memory device includes a number of memory cells. A DRAM device operates by storing charge on a capacitor at each memory location. Ultimately, the capacitor loses the charge over time and therefore needs to be periodically refreshed to its original level, a 1 or 0. All of the memory cells must be refreshed within one~~The~~ refresh period, t_{REF}, which may be for example 64 ms. Refreshing is accomplished by doing a row access for every row in the memory device. In a refresh cycle, all of the capacitors in one or more rows are first read, and then written back to, restoring full charge to the capacitor. The rows and columns of a DRAM device may be partitioned into multiple banks to reduce the large DRAM arrays into smaller segments.

In typical DRAMs, data is not directly transmitted from the storage cells. Rather, data may be transferred to sense amplifiers prior to transmission. The sense amplifiers may only store one row of data. If an operation is to be performed on a row of data other than the currently accessed row, two operations must be performed. The first operation, a precharge operation, occurs when pairs of bit lines within the memory are equalized to a midpoint voltage level. Secondly, a sense operation occurs when data in the row on which the operation is to be performed is transferred to the sense amplifiers. The DRAM device is said to be in a closed state

between the precharge operation and the subsequent sense operation. At all other times, the DRAM is said to be in an open state.

A row access operation is performed in four steps. First, a row is opened, or turned on, in the sense operation. Turning on a row of transistors that connect one row of storage cells to one row of sense amps has the effect of draining most of the charge from the storage cells, which in turn moves the bit lines slightly away from their precharged neutral level. Second, after the sense amps have reached their stable level, another set of transistors are turned on which allow the sense amps to re-drive full data levels (0 or 1) on to the bit lines. The storage cells are also restored (refreshed) to their full levels. Third, the transistors that connect the storage cells to the bit lines are shut off, and the page is considered closed. Finally, the bit lines are returned to their neutral Vdd/2 voltage by performing the precharge operation, using a precharge equalization transistor. If a refresh operation is performed, there is no need to select a particular bit with a column address. Further, data is not read at the pins of the device.

The 16 Mb generation of DRAM consisted of a single bank of memory, so that each refresh command would cause one row of the DRAM to be refreshed. With the introduction of the 64 Mb generation of synchronous DRAM (SDRAM), devices with four banks became available. DRAM performance was improved because a large degree of concurrency was allowed between the banks. The 64 Mbse DRAM were designed so that each refresh command would refresh 4 rows of memory, one row in each bank. The time to perform the 4 refreshes, t_{RFC} = 72-80 ns, was longer than the time for a single activate plus read/write cycle, to allow the refreshes to be staggered internally. The staggering prevents the large current spike that would occur if all banks were refreshed at exactly the same time. For the 64 Mb SDRAM, the refresh period t_{REF} was 64ms, while the average time between refreshes t_{REFI} was 15.6 us.

The 4-bank 256 Mb generation of double data rate SDRAM (DDR SDRAM) doubled the size of the row (the page size) relative to the 64 Mb generation, from 512B to 1 KB, and doubled the number of rows (8192) in the device relative to the 64 Mb generation (4096), but left the basic operation unchanged: each refresh command caused one row of each bank to be refreshed. Since twice as many rows needed to be refreshed in the refresh period t_{REF} (64ms), the average time between refreshes (the refresh interval) t_{REFI} was reduced from 15.6 us to 7.8 us, in going from the 64 Mb to the 256 Mb generation.

The 4-bank 512 Mb generation of DDR SDRAM doubled the size of each row relative to the 256 Mb generation, from 1 KB to 2 KB. Compared to the 256 Mb generation, the refreshes are the same – each refresh command refreshes all four banks, with a refresh interval t_{REFI} of 7.8 us. The larger page size does require a larger current to perform the refresh.

For the 4-bank 256 Mb generation, DDR and DDR2 (second generation) SDRAM have the same number of rows and banks, the same page size, and the same refresh requirements. However, starting with the 4-bank 512 Mb generation, DDR2 SDRAM has been defined with a different combination of page size, number of rows, and number of banks, compared to DDR SDRAM. The 4-bank 512 Mb generation of DDR2 SDRAM ~~gets~~achieves its doubling of capacity by doubling the number of rows in each bank (16384), while leaving the page size fixed at 1 KB. Each refresh command causes two rows to be refreshed in each bank of memory. This is possible because ~~of~~ there are actually multiple sets of sense amplifiers in each bank of memory. The maximum number of rows of a bit line inside the DRAM is physically limited to around 512 (2^9 bits). A DDR2 512 Mb SDRAM has 14 row bits, which means there are 2^(14-9) = 32 sets of sense amplifiers in each bank. These 32 sets are logically wired together to form one bank, so that reading or writing is normally only allowed to one row of a bank at a

time. Allowing two sets of sense amplifiers within the same bank to be used to refresh two rows within the same bank at mostly the same time may require a small change to the circuitry that connects the 32 sets of sense amplifiers. The total time for the refresh, t_{RFC} (105 ns), is increased.

The 8-bank 1 Gb generation ~~gets~~achieves its doubling of capacity by doubling the numbers of banks, from 4 to 8, so that each refresh command must cause ~~2~~two rows to be refresheds in each bank to be refreshed, with a total of 16 rows to be refreshed for each refresh command. The total time for the refresh, t_{RFC} (127.5 ns), is increased to keep the current requirements roughly the same as the 512 Mb generation.

The 8-bank 2 Gb generation achieves~~gets~~ its doubling of capacity by doubling the number of rows in each bank (32768), so that each refresh command must cause 4 rows to be refresheds in each bank to be refreshed, with a total of 32 rows to be refreshed for each refresh command. The total time for the refresh, t_{RFC} (195 ns), is also increased to keep the current requirements roughly the same as the 1 Gb generation.

The memory industry has not yet decides how the 4 Gb generation will ~~get~~achieve its doubling of capacity – it can be achieved by doubling either the page size, the number of rows, or the number of banks. If the refresh current is to stay roughly the same for the 4 Gb generation, ~~then~~ there will be either ~~be~~ an increase in t_{RFC} or a decrease in t_{REFI}, relative to the 2 Gb generation.

As the number of storage cells per memory bank, and the number of memory banks per device increases, the number of refresh commands issued by a memory controller ~~also~~ increases, and the proportion of time spent refreshing the memory increasess. This ultimately results in a refresh overhead that unacceptably impacts the performance of normal memory

accesses. In order to reduce refresh overhead, it may be desirable to refresh a fraction of the banks for each refresh command. This approach may be called partial multibank refresh. With a given refresh command, a fraction of the banks may be either simultaneously or sequentially refreshed. To maximize overall system performance it may be more desirable to refresh banks simultaneously in order to minimize the time that bank resources are tied up. Additionally, as DRAM devices become larger, the time required from the refresh command until the next command, the AUTO-REFRESH command period t_{RFC}, grows substantially. The impact of increased t_{RFC} is an increase in the read latency of read requests that occur during the refresh itself. For a DRAM device with a larger number of banks, there will be times when the read and write activity is skewed to one portion or another of the DRAM. Performance may be improved if refreshes are done opportunistically to the portion of the DRAM not in use, with concurrent read or write operation to the remaining portion of the DRAM.

As microprocessor speed increases, memory access speed must also increase. At the same time, the number of memory banks per memory device continues to increase, for example from four banks to eight banks to sixteen banks. Using current DRAM technology, the refresh command causes all of the banks of the DRAM to be refreshed. With multi-bank memories more locations need to be refreshed at any given time, and refreshing draws more power in a shorter time for the larger multi-bank memories. Therefore, either the current required for an all-bank refresh operation will be roughly double, for example, for eight banks as compared to four banks, or the time required to perform the refresh operation will be approximately twice as long compared to the four bank refresh. Thus, current spikes can cause significant noise problems on the power line during a refresh operation, and a longer refresh will increase the latency of any reads that are waiting for the refresh to complete. ~~Accordingly, current refresh protocols limit~~

~~refreshing to one row at a time in order to control refreshing noise.~~ What is needed is a partial refresh command that refreshes additional ~~more than one~~ rows of a bank ~~at a time~~ and a fraction of the banks of a DRAM ~~device~~ per command.

Brief Description of the Drawings

FIG. 1 illustrates a block diagram of a computer system suitable for use with an embodiment of the invention;

FIG. 2 illustrates a block diagram of a SDRAM according to an embodiment of the present invention;

FIG. 3 is a timing diagram illustrating an auto refresh operation;

FIG. 4 illustrates a block diagram of a refresh counter according to an embodiment of the present invention;

FIG. 5 illustrates using an all bank refresh command to refresh 16 rows according to an embodiment of the present invention;

FIG. 6 illustrates using an upper/lower half bank refresh command to refresh 8 rows according to an embodiment of the present invention;

FIG. 7 illustrates using an upper/lower half bank refresh command to refresh 16 rows according to an alternative embodiment of the present invention; ~~and~~

FIG. ~~5~~ 8 illustrates a flow chart diagram of a partial bank refresh to a portion of the banks occurring along with an activate operation followed by a read or write operation according to an embodiment of the present invention; and

FIG. 9 illustrates a memory controller according to an embodiment of the present invention.

Detailed Description

The present invention improves the performance of memory subsystems by providing a method to refresh a fraction of the banks in a DRAM in response to a given refresh command. Refreshing a fraction of the banks allows a degree of concurrency with reads and/or writes to the remaining banks in the DRAM which are not being refreshed. Additional performance may be gained because it is not necessary to close the pages of the banks that are not being refreshed, potentially reducing the read latency to the data in those banks. In embodiments of the present invention each refresh command refreshes half of the banks in the DRAM. For example, ~~I~~in one embodiment, each refresh command (refreshing half of the banks in the DRAM) does half as much work as an all-bank refresh command (for the same number of rows per bank), so that twice as many refresh commands are needed per refresh period t_{REF}. In a second embodiment, the number of refresh commands per refresh period t_{REF} stays the same as an all bank refresh, so that each refresh command refreshes twice as many rows per bank (as compared with the all bank refresh), thereby accomplishing~~doing~~ as much work per refresh command as an all-bank refresh command would.

As discussed above, DRAM devices require periodic refresh operations to retain data in its storage cells. A refresh operation consists of a row sense operation and a row precharge operation. Each memory cell needs to be refreshed within the refresh period t_{REF}. A typical t_{REF} value may be 64 ms. Therefore, each row in each memory bank needs to be refreshed within t_{REF}.

As the number of banks per memory device increases and as the number of devices in memory systems increases, the number of precharge and refresh commands issued by a memory controller also increases. This ultimately results in a precharge and refresh overhead that

unacceptably impacts the performance of normal memory accesses as measured by effective data bandwidth and memory access latency.

As discussed above, a problem caused by all-bank refreshing is the generation of current spikes. Each refresh operation for each bank requires a certain amount of supply current over time. For a row sense operation there is a large initial spike because the row sensing circuits have been designed to access cell data as quickly as possible in order to minimize the latency. With all-bank refreshing, multiple banks simultaneously conduct a row sense, thus, the current spike effect may be additive causing greater probability of circuit failure.

The present invention implements refreshing a fraction of the banks for each refresh command to reduce refresh overhead on the memory system bus. This approach is called partial multibank refreshing. With a given refresh command, either a fraction of the banks are simultaneously refreshed, or a fraction of the banks are sequentially refreshed from the same command. To maximize overall system performance it may be more desirable to refresh banks simultaneously in order to minimize the time that bank resources are tied up. Within each bank, it is also desirable to refresh multiple rows, either simultaneously or in a staggered fashion.

In an embodiment of the present invention, the generation of row and bank addresses during refresh is split between on-chip and external commands. A row counter is provided on the memory chip, with the row counter being used for refresh operations, both normal and self-refresh. Only the bank address needs to be sent over the memory bus.

FIG. 1 is a block diagram of a computer system suitable for use with the invention. Computer system 100 comprises bus 101 or other device for communicating information, and processor 102 coupled with bus 101 for processing information. Computer system 100 further includes synchronous dynamic random access memory (SDRAM) or other dynamic storage

device 104 (referred to as main memory), coupled to bus 101 for storing information and instructions to be executed by processor 102. Main memory 104 also can be used for storing temporary variables or other intermediate information during execution of instructions by processor 102. Computer system 100 also comprises read only memory (ROM) and/or other static storage device 106 coupled to bus 101 for storing static information and instructions for processor 102. Data storage device 107 is coupled to bus 101 for storing information and instructions.

Data storage device 107 such as magnetic disk or optical disc and corresponding drive can be coupled to computer system 100. Computer system 100 can also be coupled via bus 101 to display device 121, such as a cathode ray tube (CRT) or liquid crystal display (LCD), for displaying information to a computer user.

Alphanumeric input device 122, including alphanumeric and other keys, is typically coupled to bus 101 for communicating information and command selections to processor 102. Another type of user input device is cursor control 123, such as a mouse, a trackball, or cursor direction keys for communicating direction information and command selections to processor 102 and for controlling cursor movement on display 121.

In one embodiment, processor 102 and one or more of the components coupled to bus 102, such as main memory 104, are source synchronous components. Of course, any one or more components of computer system 100 can be source synchronous. Thus, computer system 100 can be either a partially source synchronous or fully source synchronous environment. In one embodiment, computer system 100 is a differential-strobe source synchronous system in which complementary strobe signals are communicated in parallel with data signals over the bus.

Alternatively, computer system 100 is a single-strobe source synchronous system in which a single strobe signal is communicated in parallel with data signals over the bus.

A synchronous dynamic random access memory (SDRAM) according to embodiments of the present invention is illustrated generally at 200 in FIG. 2 in block diagram form. The present invention is not limited to SDRAMs, as the present invention is equally applied to other types of memory devices. Only the circuitry relevant to the current discussion is shown. As illustrated in FIG. 2, SDRAM 200 may include 8 memory bank arrays, a bank 0 memory array 220 up to a bank 7 memory array 227 which all comprise storage cells organized in rows and columns for storing data.

A system clock (CLK) signal is provided through a CLK input pin and a clock enable signal (CKE) is provided through a CKE input pin to SDRAM 200. The CLK signal is activated and deactivated based on the state of the CKE signal. All the input and output signals of SDRAM 200, with the exception of the CKE input signal during power down and self refresh modes, are synchronized to the active going edge of the CLK signal (See also FIG. 3).

A chip select (CS*) input pin inputs a CS* signal which enables, when low, and disables, when high a command decoder 260. The command decoder 260 is included in a command controller 280. The command decoder 260 receives control signals including a row access strobe (RAS*) signal on a RAS* pin, column access strobe (CAS*) signal on a CAS* pin, and a write enable (WE*) signal on a WE* pin. The command decoder 260 decodes the RAS*, CAS*, and WE* signals to place the command controller 280 in a particular command operation sequence. The command controller 280 controls the various circuitry of SDRAM 200 based on decoded commands such as during controlled reads or writes from or to bank 0 memory array 220 through bank 7 memory array 227. Bank address signals (BA0, BA1, BA2) are provided on

separate BA input pins to define which of at least one memory bank array should be operated on by certain commands issued by the command controller 280.

Address inputs bits are provided on input pins A0-AN. Current DDR and DDRII specifications define up to 16 address pins, AO-A15. For example, 1 Gb SDRAM devices use input pins A0-A13. The row and column address input bits are multiplexed on the address input pins. During write transfer operations, data is supplied to SDRAM 200 via input/output pins (DQ1-DQ4). During read transfer operations, data is clocked out of SDRAM 200 via input/output pins DQ1-DQ4.

SDRAM 200 must be powered-up and initialized in a predefined manner. In addition, all memory bank arrays 220-227 must be precharged and placed in an idle state. The precharging of the memory bank arrays is preformed with a precharge command operation.

Two refresh commands are typically available in SDRAM 200, an AUTO-REFRESH command and a SELF-REFRESH command. The AUTO-REFRESH command is performed with a refresh controller 240 and a refresh counter 245 in a manner described below to refresh the memory bank arrays 220-227. The SELF-REFRESH command is performed with the refresh controller 240, a self-refresh oscillator and timer 260, and the refresh counter 245. The self-refresh oscillator and timer 260 internally generates a clock signal to provide internal timing for refreshes which occur in self-refresh mode.

An AUTO-REFRESH command is initiated by registering CS*, RAS* and CAS* low with WE* high. The AUTO-REFRESH command is non-persistent, and therefore must be issued each time a refresh is required. Addressing of the rows is generated by internal refresh controller 240 and refresh counter 245. Thus, the A0-AN address inputs are treated as "don't care" conditions during an AUTO-REFRESH command. In one embodiment of the SDRAM

200 (256 Mb DDR2) having 8192 rows, all 8192 rows need to be refreshed every 64 ms. Therefore, providing a distributed AUTO-REFRESH command approximately every 7.8 microseconds meets this refresh requirement and ensures that each row is refreshed.

An auto refresh operation in one embodiment of SDRAM 200 performed in a memory bank array specified by the BA signals (BA0, BA1, BA2) during auto refresh mode is illustrated in timing diagram form in FIG. 3. As indicated in FIG. 3, each auto refresh operation in this embodiment of SDRAM 200 is to at least one memory bank array specified by the state of the BA signals (BA0, BA1, BA2) provided on the BA pins.

Preferably, the AUTO-REFRESH commands are alternated between banks. However, more than one row in each of the specified banks may be auto refreshed before switching banks. In an embodiment of the present invention, refresh counter 245 counts partially through the rows of the at least one specified bank ~~then~~ before a memory controller switches to other banks. In this embodiment, refresh counter 245 preferably counts through a specified number of rows from 0 to N prior to the memory controller switches~~ing~~ banks. For example, in one embodiment, refresh counter 245 provides addresses for row 0 of the specified banks, then row 1 of the specified banks, then row 2 of the specified banks, . . . , and finally row N of the specified banks of SDRAM 200. In this embodiment, once at least one memory bank array is auto refreshed, some combination of the other memory bank arrays can be auto refreshed. The number of rows N per bank refreshed per AUTO-REFRESH command can be calculated from DRAM timing specifications:

Rows per refresh = Rows per bank*Number of banks* t_{REFI} / t_{REF}

t_{REFI} = average interval between refresh commands

t_{REF} = Refresh Period

For example referring to FIG. 5, for an all bank refresh of a 1 Gb DDRII DRAM having 8 banks, 16384 rows per bank, t_{REFI} = 7.8 us, and t_{REF} = 64 ms.

Rows per refresh = 8 * 16384 * 7.8 us / 64 ms = 16 (Each bank will have two rows refreshed per refresh command). If refreshing a row takes approximately t_{RC} = 60 ns, and the row refreshes are staggered by about 4 ns, then a 1 Gb DDR2 refresh command would take 60 + 15 * 4 = 120 ns, roughly consistent with the DDR2 specification of 127.5 ns~~Note that 8 refreshes for a DDRII 1 Gb DRAM are spread out, one started every 7.5 ns~~. Using the all bank refresh requires 8192 refresh commands per t_{REF} = 64 ms. Note that the rows are refreshed in a staggered fashion per refresh command to prevent the large current spike that would occur if all rows were refreshed at exactly the same time. Table A includes data for various other DRAM devices.

TABLE A

DDR2 DRAM Size	Banks	Rows/refresh	t_{RFC}	row per bank per refresh
256 Mb	4	4	75 ns	1
512 Mb	4	8	105 ns	2
1 Gb	8	16	127.5 ns	2
2 Gb	8	32	195 ns	4

A refresh counter 245 employed in one embodiment of SDRAM 200 is illustrated in block diagram form in FIG. 4. This embodiment of SDRAM 200 includes a separate refresh counter portion for each memory bank array in the SDRAM. For example, as illustrated in FIG. 4, refresh counter 245 includes a refresh counter bank 0 portion 245A and a refresh counter bank

1 portion 245B, up to a refresh counter bank 7 portion 245H. If each memory bank array has ~~16382~~ 16384 rows, each refresh counter bank portion includes 14 bits to hold the existing row address currently being refreshed. This is in contrast to a single portion counter 245 which has one counter portion with 14 bits to address the 16382 rows of every memory bank array.

By having a refresh counter portion dedicated to each bank, the auto refresh operation can stop partially through the refreshing of rows in a given specified bank. For example, an auto refresh operation can be performed for row 0 through row 4 in bank 0, then switch to bank ~~1~~ 4 to perform auto refreshes on row 0 through row 4 in bank 4~~addressed rows~~. When the auto refresh operation returns to bank 0, the count held in refresh counter bank 0 portion 245A indicates that the refreshing was last performed on row 4 of bank 0, so that refreshing then begins in row 5 or whatever row was due to be refreshed prior to switching banks.

An auto refresh operation may be performed on at least one specified memory bank array of an SDRAM 200 using BA signals (BA), BA1, BA2) during auto refresh mode as described in more detail below. In embodiments of the present invention, other commands can be performed on the memory bank arrays not being refreshed.

A new "partial refresh command" is defined in Table B for an SDRAM with eight banks. For these eight bank SDRAM parts, a refresh command with BA2 driven low will cause the lower four banks of the DRAM to be refreshed. A refresh command with BA2 driven high will cause the upper four banks of the DRAM to be refreshed. Although this multibank addressing scheme naturally supports the most straight-forward sequential address assignment to banks, other assignments are applicable.

TABLE B

BA0	BA1	BA2	Refreshed Bank(s)
DON'T CARE	DON'T CARE	Low[1]	Banks 0 ~ 3
DON'T CARE	DON'T CARE	High	Banks 4 ~ 7

Note 1: BA2 = DON'T CARE for four bank devices

The advantages of the present invention are two fold. The power drawn by the upper or lower bank refresh on the eight bank part will be the same as the power drawn by an "all bank" refresh on a four bank part, without requiring the refresh period to be extended in time. This eliminates the problem that refreshing eight banks simultaneously would ordinarily cause an instantaneous current draw that exceeds the limits of the package and die.

In addition, the upper/lower refresh command allows half of the banks to remain open and accessible for reads and writes during the refresh of the other half of the banks. Furthermore, the refresh time is left equal to the refresh time for a four bank device, minimizing the chance of a large queue of read requests to be waiting for the refresh to complete.

An additional embodiment of the present invention defines the partial refresh command to cause either one fourth of the banks to be refreshed, or optionally, one half of the banks to be refreshed. Table C below indicates how such a command is implemented for an 8-bank SDRAM. Again, this multibank addressing scheme naturally supports the most straight-forward sequential address assignment to banks, other assignments are applicable.

TABLE C

BA0	BA1	BA2	Refreshed Bank(s)
LOW	LOW	LOW	Banks 0 ~ 2
LOW	HIGH	LOW	Banks 1 ~ 3
HIGH	LOW	LOW	Banks 4 ~ 5
HIGH	HIGH	LOW	Banks 6 ~ 7
LOW	LOW	HIGH	Banks 0 ~ 3
HIGH	LOW	HIGH	Banks 4 ~ 7
DON'T CARE	HIGH	HIGH	Reserved

The present invention is extendable to a 16-bank SDRAM. The general case is a refresh command that causes "M banks" to be refreshed on an "N bank" DRAM.

FIG. 9 illustrates a memory controller according to an embodiment of the present invention. Memory controller 900 maintains separate work queues, upper bank work queues 910 and lower bank work queues 920 for each bank of the SDRAM 200 . The memory controller 900 may also maintain refresh counter portions 945A-945H for each memory bank array in the SDRAM 200. The refresh counter portions 945A-945H may be organized into upper bank counters 945E-945H and lower bank counters 945A-945E. Memory controller 900 may utilize upper bank counters 945E-945H and lower bank counters 945A-945E to keep track of upper bank refreshes separately from lower bank refreshes. Memory controller 900 may also utilize an upper bank refresh scheduler 950 and a lower bank refresh scheduler 960. The upper bank refresh scheduler 950 and the lower bank refresh scheduler 960 may operate utilizing a credit or debit model.

For example, either scheduler 950, 960 may have a counter with a maximum count of 8 that is incremented each time a refresh occurs, and decremented every tREFI nsec. If the counter = 8, then no more refreshes are needed for a specified time. If the counter = 0, then a priority refresh has to occur (upper or lower). If the counter is between 1 and 7, then a refresh can be scheduled opportunistically whenever the upper empty signal 911 or lower empty signal 921 are asserted.

~~I~~In embodiments of the present invention, the~~a~~ memory controller 900 in communication with the SDRAM 200~~memory device~~ may keep track of in which bank the AUTO-REFRESH command is being performed. In an eight bank system, the knowledge of the current banks being refreshed may be maintained by the memory controller 900. The memory controller 900 specifies the bank(s) to be refreshed at the initiation of an AUTO-REFRESH command with the BA signals (BA0, BA1, BA2) on the BA pins in a eight memory bank device. In embodiments

of the present invention, only the banks specified to be refreshed need to be idle at a given time. Thus, other commands may be performed on other banks not being refreshed during an auto refresh operation on the specified banks. Other embodiments of the present invention may include restrictions as to which DRAM commands may be performed concurrently with the refresh command, or concurrently during a specified phase of the refresh cycle t_{RFC}. For example, reads, writes and precharges may be allowed, but activate may be disallowed, in which case, pages must be left open in order for work to be done during the partial bank refresh.

The t_{RFC} time, shown in FIG. 3, representing the command period from a refresh to a refresh or from a refresh to an ACTIVE command can be utilized to perform commands in banks not being refreshed. For example, the auto refreshing of the banks 0-3 memory arrays while an active and a read operation are performed in the bank ~~1~~-4 memory array is illustrated in timing diagram form in FIG. 3 and graphically illustrated in FIG. 6 and FIG. 7. As illustrated in FIG. 3, an auto refresh command is started by specifying banks 0-3 using the "lower bank refresh command" i.e., a refresh command with BA2 driven low will cause the lower four banks of the SDRAM to be refreshed ~~as the specified memory bank array to be refreshed~~. Subsequently, an ACTIVE command is started in bank ~~1~~-4 to activate the rows of the bank ~~1~~-4 memory array. As illustrated in FIG. 6, the concurrent operation initiated by the ACTIVATE command to bank 4 begins after approximately 45 ns. FIG. 7 illustrates the concurrent operation initiated by the ACTIVATE command to bank 4 begins after approximately 80 ns. A read command with a read latency of two is then performed to read data out from ~~column m~~column n of the activated row. This transfer operation is performed before an auto refresh command is started by

specifying banks 4-7 using the "upper bank refresh command" i.e., a refresh command with BA2 driven high will cause the upper four banks of the SDRAM to be refreshed.

~~tween two AUTO-REFRESH commands to bank 0. Although the ACTIVE command is shown after the AUTO-REFRESH command, the ACTIVE command to bank 1 could be performed before the first AUTO-REFRESH command illustrated in FIG. 3.~~

FIG. 3 shows an ACTIVE command and a READ command, but it will be understood that a write operation which writes data into SDRAM 200 or other operation could also be performed between the two AUTO-REFRESH commands during the t_{RFC} time. In addition, the read operation is shown for one column of data, but may be extended to apply to a burst of length two, four, eight, or full page if the operation could be performed in between the two AUTO-REFRESH commands in the time represented by t_{RFC}. The embodiments of SDRAM 200 described above refer to an eight memory bank device, but the present invention applies to any multi-bank synchronous memory device such as a sixteen bank memory device.

FIG. 5 illustrates using an all bank refresh command to refresh 16 rows according to an embodiment of the present invention. For example, a 1 Gb, 8 bank DDR2 SDRAM 200 is refreshed by an all bank refresh command where 2 rows per bank are refreshed per refresh command. FIG. 5 illustrates that during the time t_{RFC} = 127.5 ns, 2 rows per bank, row a and row b, for banks 0-7 are refreshed in a staggered fashion. Note that no concurrent operations take place. Thus, 8192 refresh commands are issued by the memory controller 900 per t_{REF} = 64 ms.

FIG. 6 illustrates using a lower half bank refresh command to refresh 8 rows according to an embodiment of the present invention. For example, a 1 Gb, 8 bank DDR2 SDRAM 200 is refreshed by a lower half bank refresh command where 2 rows per bank are refreshed per refresh command for 4 banks. FIG. 6 illustrates that during the time t_{RFC} = 90 ns, 2 rows per bank, row a

and row b, for banks 0-3 are refreshed in a staggered fashion. For this embodiment twice as many refresh commands (16,384) would be required as compared to the all bank refresh (8192) described above to refresh all the rows in all 8 banks in t_{REF} = 64 ms. However, note that concurrent operations on banks 4-7 is achievable after approximately 45 ns and lasting for approximately 45 ns. The 45 ns delay period allows all 8 rows to begin the refresh operation before concurrent operations begin. This is required to prevent the concurrent operations, such as an activate operation which draws significant current, to occur during the beginning of a refresh operation. Also note that the rows are refreshed in a staggered fashion per refresh command to prevent the large current spike that would occur if all rows were refreshed at exactly the same time.

FIG. 7 illustrates using a lower half bank refresh command to refresh 16 rows according to an alternative embodiment of the present invention. For example, a 1 Gb, 8 bank DDR2 SDRAM 200 is refreshed by a lower half bank refresh command where 4 rows per bank are refreshed per refresh command. FIG. 7 illustrates that during the time t_{RFC} = 127.5 ns, 4 rows per bank, rows a, b, c, and d for banks 0-3 are refreshed in a staggered fashion. For this embodiment an equal number of refresh commands (8192) would be required as compared to the all bank refresh (8192) described above to refresh all the rows in all 8 banks in t_{REF} = 64 ms. However, note that concurrent operations on banks 4-7 is achievable after approximately 80 ns and lasting for approximately 50 ns. The 80 ns delay period allows all 16 rows to begin the refresh operation before concurrent operations begin. Again, this is required to prevent the concurrent operations, such as an activate operation which draws significant current, to occur during the beginning of a refresh operation. Also note that the rows are refreshed in a staggered

fashion per refresh command to prevent the large current spike that would occur if all rows were refreshed at exactly the same time.

The embodiments shown in FIG 6 and FIG 7 illustrate the tradeoff between using twice as many refresh commands to achieve a shorter time period before concurrent operations are allowed to begin (45 ns) versus an equal number of commands (compared to the all bank refresh) resulting in a longer time period before concurrent operations are allowed to begin (80 ns).

FIG. ~~5~~ 8 illustrates a flow chart diagram of a partial bank refresh to a portion of the banks occurring along with an activate operation followed by a read or write operation to a portion of the banks not being refreshed. The SDRAM 200 receives ~~500~~ 800 control signals including a row access strobe (RAS*) signal on a RAS* pin, column access strobe (CAS*) signal on a CAS* pin, and a write enable (WE*) signal on a WE* pin. The command decoder 260 decodes ~~505~~ 805 the RAS*, CAS*, and WE* signals to place the command controller 280 in a particular command operation sequence. The command controller 280 will initiate ~~510~~ 810 an AUTO-REFRESH command if registering CS*, RAS* and CAS* low with WE* high. The command decoder 260 determines ~~515~~ 815 the bank(s) to be refreshed using bank address signals (BA0, BA1, BA2) received on the plurality of bank address lines. The command controller 280 precharges ~~520~~ 820 the memory bank(s) to be refreshed to place them in an idle state. The internal refresh controller 240 and refresh counter 245 specific to bank(s) being refreshed determines ~~525~~ 825 the row(s) to be refreshed. The selected row(s) of selected bank(s) is/are refreshed ~~530~~830. The refresh counter for the bank refreshed is incremented ~~535~~835.

In addition, other commands may be performed on other banks not being refreshed during an auto refresh operation on the banks specified to be refreshed. The SDRAM 200 receives ~~500~~ 800 control signals including a row access strobe (RAS*) signal on a RAS* pin,

column access strobe (CAS*) signal on a CAS* pin, and a write enable (WE*) signal on a WE* pin. The command decoder 260 decodes ~~505~~ 805 the RAS*, CAS*, and WE* signals to place the command controller 280 in a particular command operation sequence. The command controller 280 may initiate ~~550~~ 850 an ACTIVATE command to a bank not being refreshed if registering CS*, CAS* low with RAS* and WE* high. The command decoder 260 determines ~~555~~ 855 the bank to be activated using bank address signals (BA0, BA1, BA2) received on the plurality of bank address lines and determines the row to be activated using address signals (A0-AN) received on the address lines. The command controller 280 may initiate ~~560~~ 860 a READ command if registering CS*, CAS* low with RAS* and WE* high. Alternatively, the command controller 280 may initiate ~~560~~ 860 a WRITE command if registering CS*, CAS*, and WE* low with RAS* high. The command decoder 260 determines ~~565~~ 865 the bank to be read or written to using bank address signals (BA0, BA1, BA2) received on the bank address lines and determines the column(s) to be read or written to using address signals (A0-AN) received on the address lines. The SDRAM 200 then performs the read or write operation.

While the description above refers to particular embodiments of the present invention, it will be understood that many modifications may be made without departing from the spirit thereof. The accompanying claims are intended to cover such modifications as would fall within the true scope and spirit of the present invention. The presently disclosed embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims, rather than the foregoing description, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

What is claimed is:

1. -A method of operating a memory device having multiple memory bank arrays and being responsive to command signals and a plurality of bank address signals, the method comprising:

specifying at least one of a multiple of memory bank arrays to be refreshed using a plurality of bank address signals; and

initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays.

2. -The method of claim 1, wherein the specified at least one of the multiple memory bank arrays is specified in logic based on the plurality of bank address signals received.

3. -The method of claim 1 further comprising:

initiating, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command signal controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed.

4. -The method of claim 1, wherein multiple rows per memory bank array are refreshed per auto-refresh command.

5. The method of claim 1, wherein multiple rows per memory bank array are refreshed in a staggered fashion per auto-refresh command.

~~5~~6. -The method of claim 1, wherein the method is performed using a synchronous dynamic random access memory device.

7. The method of claim 3, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations.

~~6~~8. -An article comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following

specifying at least one of a multiple of memory bank arrays to be refreshed using a plurality of bank address signals; and

initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays.

~~7~~9. -The article according to claim ~~6~~8, wherein the specified at least one of the multiple memory bank arrays is specified in logic based on the plurality of bank address signals received.

~~8~~10. -The article according to claim ~~6~~8, further comprising:

initiating, during the auto refresh operation to the at least one of the specified memory bank arrays, a second command signal controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed.

~~9~~11. -The article according to claim ~~6~~8, wherein multiple rows per memory bank array are refreshed per auto-refresh command.

12. The article according to claim 8, wherein multiple rows per memory bank array are refreshed in a staggered fashion per auto-refresh command.

~~10~~13. -The article according to claim ~~6~~8, wherein the method is performed using a synchronous dynamic random access memory device.

14. The article according to claim 10, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations.

~~11~~15. -A memory device responsive to command signals and bank address signals, the memory

device comprising:

multiple memory bank arrays, each memory bank array having storage cells; and

a command controller/decoder responsive to selected command signals and bank address signals to initiate an auto-refresh command controlling an auto refresh operation to at least one specified memory bank array of the multiple memory bank arrays.

~~12~~16. The memory device of claim ~~11~~15, wherein the at least one specified memory bank array of the multiple memory bank arrays is determined based on which memory bank arrays have been refreshed and a subsequent known order of refreshing the memory bank arrays.

~~13~~17. The memory device of claim ~~12~~16, wherein the at least one specified memory bank array of the multiple memory bank arrays is determined based on a command specifying which bank is to be next refreshed and a subsequent known order of refreshing the memory bank arrays.

~~14~~18. The memory device of claim ~~12~~16, wherein the command controller/decoder is responsive to selected command signals to initiate during the auto refresh operation to the at least one of the specified memory bank arrays a second command controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the memory bank arrays being refreshed.

~~15~~19. The memory device of claim ~~11~~15, further comprising a refresh counter for incrementing an address of a row to be refreshed, wherein the refresh counter has a separate counter portion for each of the multiple memory bank arrays.

~~16~~20. The memory device of claim ~~11~~15, wherein multiple rows per memory bank array are refreshed per auto-refresh command.

21. The memory device of claim 15, wherein multiple rows per memory bank array are refreshed in a staggered fashion per auto-refresh command.

~~17~~22. ~~-~~The memory device of claim ~~11~~15, wherein the memory device is a synchronous dynamic random access memory.

23. The memory device of claim 18, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations.

~~18~~24. ~~-~~A method of operating a memory device having multiple memory bank arrays and being responsive to command signals and a plurality of bank address signals, the method comprising:

specifying at least one of a multiple of memory bank arrays to be refreshed using a plurality of bank address signals;

initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, wherein multiple rows per memory bank array are refreshed per auto-refresh command; and

initiating, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command signal controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed.

~~19~~25. ~~-~~The method of claim ~~18~~24, wherein the specified at least one of the multiple memory bank arrays is specified in logic based on the plurality of bank address signals received.

~~20~~26. ~~-~~The method of claim ~~18~~24, wherein multiple rows per memory bank array are refreshed in a staggered fashion per auto-refresh command. ~~wherein multiple rows per memory bank array are refreshed per auto-refresh command.~~

~~21~~27. ~~-~~The method of claim ~~18~~24, wherein the method is performed using a synchronous dynamic random access memory device.

~~22~~28. ~~The memory controller~~method of claim ~~18~~24, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations.

~~23~~29. ~~The memory controller~~method of claim ~~22~~28, wherein second command signals, to initiate an activate operation to open a page not to be refreshed, are issued by the memory controller ~~before~~ after first command signals to initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays to be refreshed, in preparation for issuing second command signals to initiate read operations or write operations to the open page.

~~24~~30. A memory controller for controlling a memory device having multiple memory bank arrays comprising:

a processor for scheduling and generating a plurality of bank address signals, first command signals, and second command signals, wherein the plurality of bank address signals specifies at least one of a multiple of memory bank arrays to be refreshed, the first command signals initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, and the second command signals initiate, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed.

~~25~~31. The memory controller of claim ~~24~~30, wherein the specified at least one of the multiple memory bank arrays is specified in logic based on the plurality of bank address signals received.

~~26~~32. -The memory controller of claim ~~24~~30, wherein multiple rows per memory bank array are refreshed per auto-refresh command.

33. The memory controller of claim 30, wherein multiple rows per memory bank array are refreshed in a staggered fashion per auto-refresh command.

~~27~~34. -The memory controller of claim ~~24~~30, wherein the memory device is a synchronous dynamic random access memory device.

~~28~~35. -The memory controller of claim ~~24~~30, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations.

~~29~~36. -The memory controller of claim ~~28~~35, wherein second command signals to initiate a second activate operation to open a page not to be refreshed are issued by the memory controller ~~before~~ after first command signals to initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays to be refreshed, in preparation for issuing second command signals to initiate read operations or write operations to the open page.

~~30~~37. -A system comprising:

a memory device having multiple memory bank arrays; and

a memory controller for controlling the memory device, including a processor for scheduling and generating a plurality of bank address signals, first command signals, and second command signals, wherein the plurality of bank address signals specifies at least one of a multiple of memory bank arrays to be refreshed, the first command signals initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, and the second command signals initiate, before or during the auto

refresh operation to the at least one of the specified memory bank arrays, a second command controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed.

~~31~~38. ~~-~~The system of claim ~~30~~37, wherein the specified at least one of the multiple memory bank arrays is specified in logic based on the plurality of bank address signals received.

~~32~~39. ~~-~~The system of claim ~~30~~37, wherein multiple rows per memory bank array are refreshed per auto-refresh command.

40. The system of claim 37, wherein multiple rows per memory bank array are refreshed in a staggered fashion per auto-refresh command.

~~33~~41. ~~-~~The system of claim ~~30~~37, wherein the memory device is a synchronous dynamic random access memory device.

~~34~~42. ~~-~~The system ~~memory controller~~ of claim ~~30~~37, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations.

~~35~~43. ~~-~~The system~~memory controller~~ of claim ~~34~~42, wherein second command signals to initiate a second activate operation to open a page not to be refreshed are issued by the memory controller ~~before~~ after first command signals to initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays to be refreshed, in preparation for issuing second command signals to initiate read operations or write operations to the open page.

ABSTRACT OF THE DISCLOSURE

A "partial refresh command" is used to refresh a fraction of the banks in a multi-bank DRAM. In a first implementation the command refreshes one half of the banks. In a second implementation the command refreshes one quarter of the banks. The power drawn by the upper or lower bank refresh on the eight bank DRAM is the same as the power drawn by an "all bank" refresh on a four bank DRAM, without requiring the refresh period to be extended.

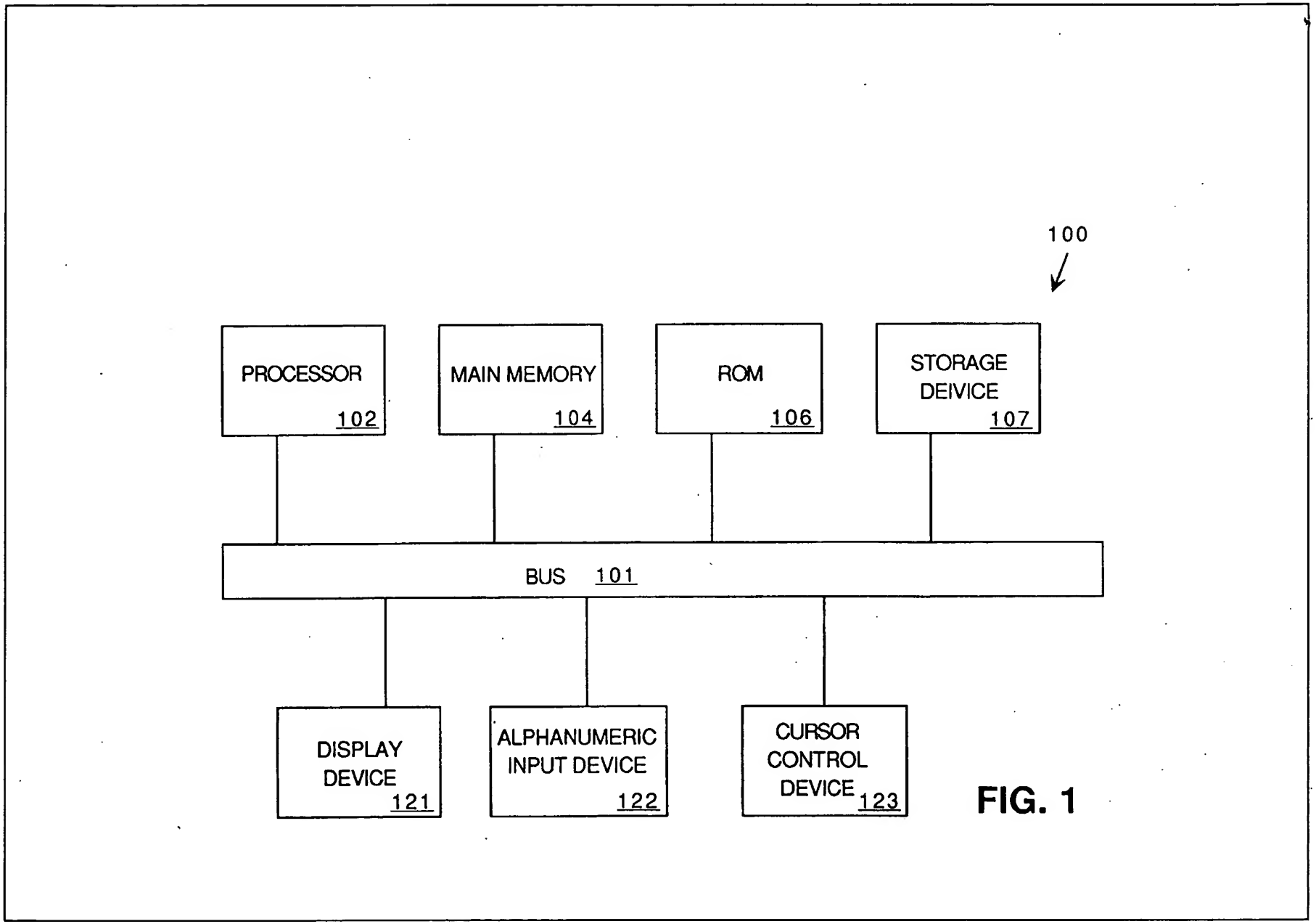
100
PROCESSOR
102
MAIN MEMORY
104
ROM
106
STORAGE
DEIVICE
107
BUS 101
DISPLAY
DEVICE
121
ALPHANUMERIC
INPUT DEVICE
122
CURSOR
CONTROL
DEVICE
123

FIG. 1

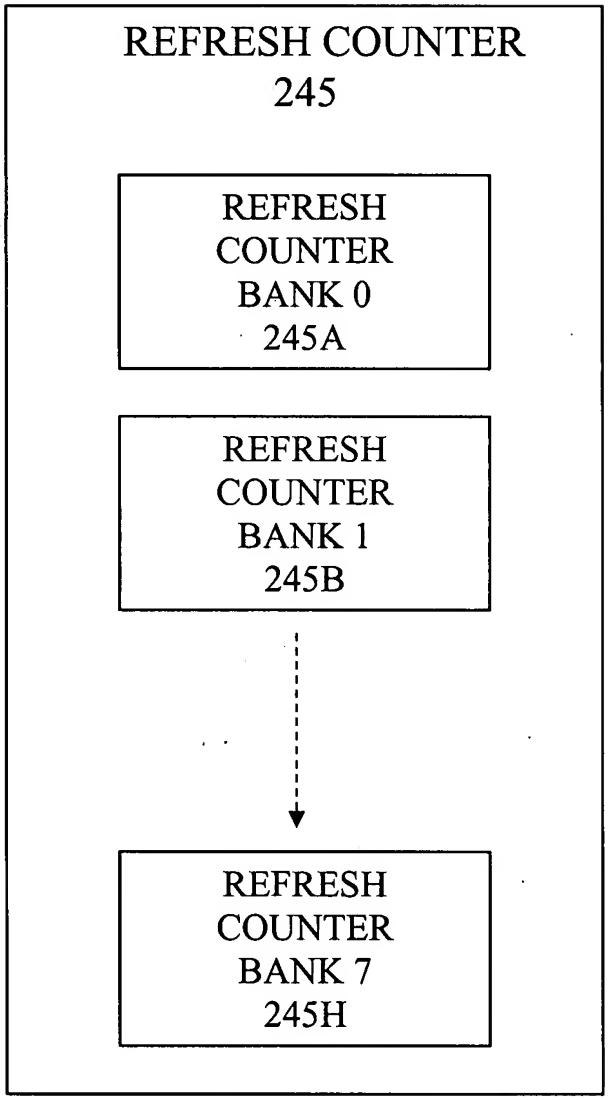
REFRESH COUNTER
245
REFRESH
COUNTER
BANK 0
245A
REFRESH
COUNTER
BANK 1
245B
REFRESH
COUNTER
BANK 7
245H

FIG. 4

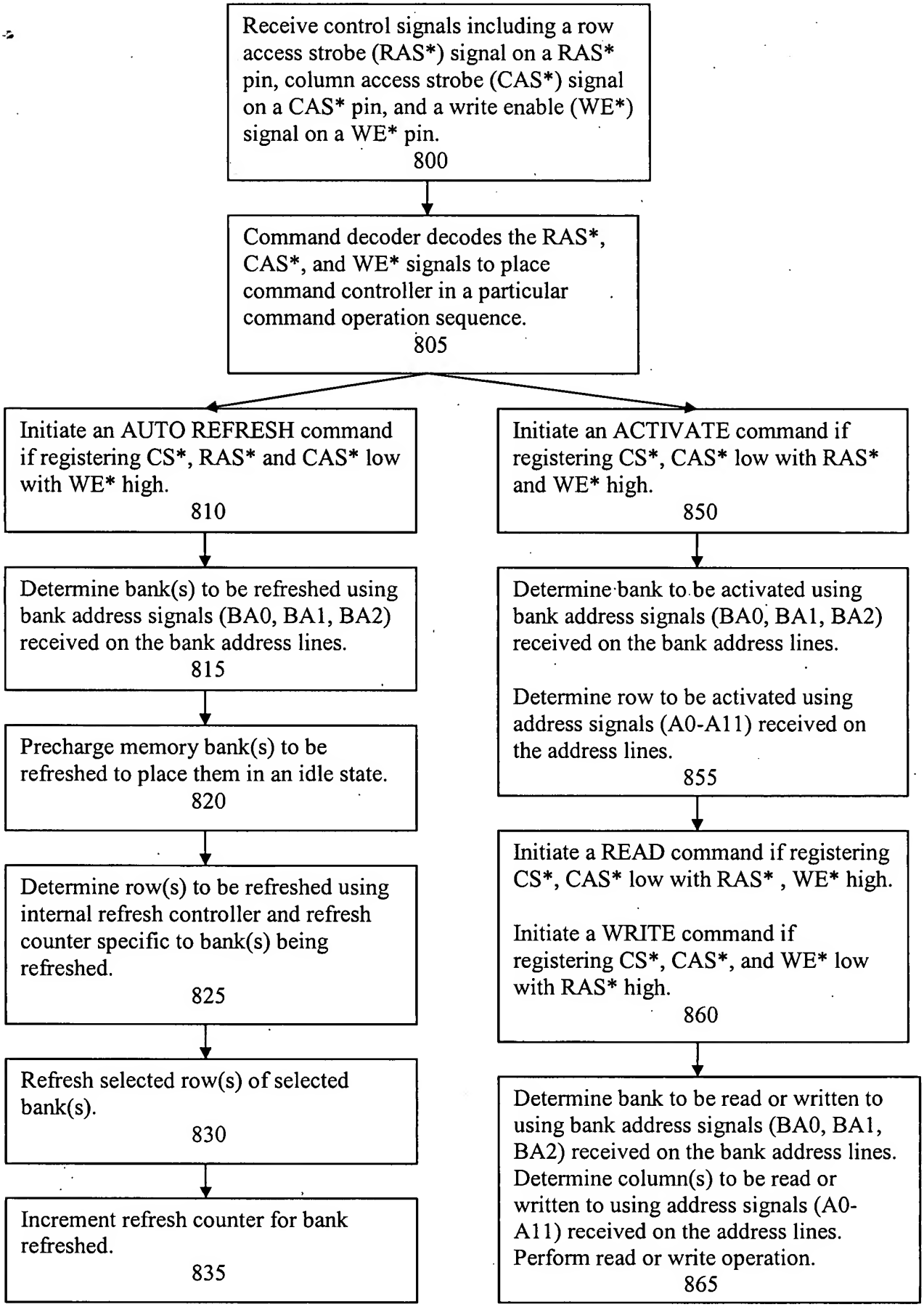
Receive control signals including a row access strobe (RAS*) signal on a RAS* pin, column access strobe (CAS*) signal on a CAS* pin, and a write enable (WE*) signal on a WE* pin.
800
Command decoder decodes the RAS*, CAS*, and WE* signals to place command controller in a particular command operation sequence.
805
Initiate an AUTO REFRESH command if registering CS*, RAS* and CAS* low with WE* high.
810
Determine bank(s) to be refreshed using bank address signals (BA0, BA1, BA2) received on the bank address lines.
815
Precharge memory bank(s) to be refreshed to place them in an idle state.
820
Determine row(s) to be refreshed using internal refresh controller and refresh counter specific to bank(s) being refreshed.
825
Refresh selected row(s) of selected bank(s).
830
Increment refresh counter for bank refreshed.
835
Initiate an ACTIVATE command if registering CS*, CAS* low with RAS* and WE* high.
850
Determine bank to be activated using bank address signals (BA0, BA1, BA2) received on the bank address lines.
Determine row to be activated using address signals (A0-A11) received on the address lines.
855
Initiate a READ command if registering CS*, CAS* low with RAS* , WE* high.
Initiate a WRITE command if registering CS*, CAS*, and WE* low with RAS* high.
860
Determine bank to be read or written to using bank address signals (BA0, BA1, BA2) received on the bank address lines. Determine column(s) to be read or written to using address signals (A0-A11) received on the address lines. Perform read or write operation.
865

FIG. 8

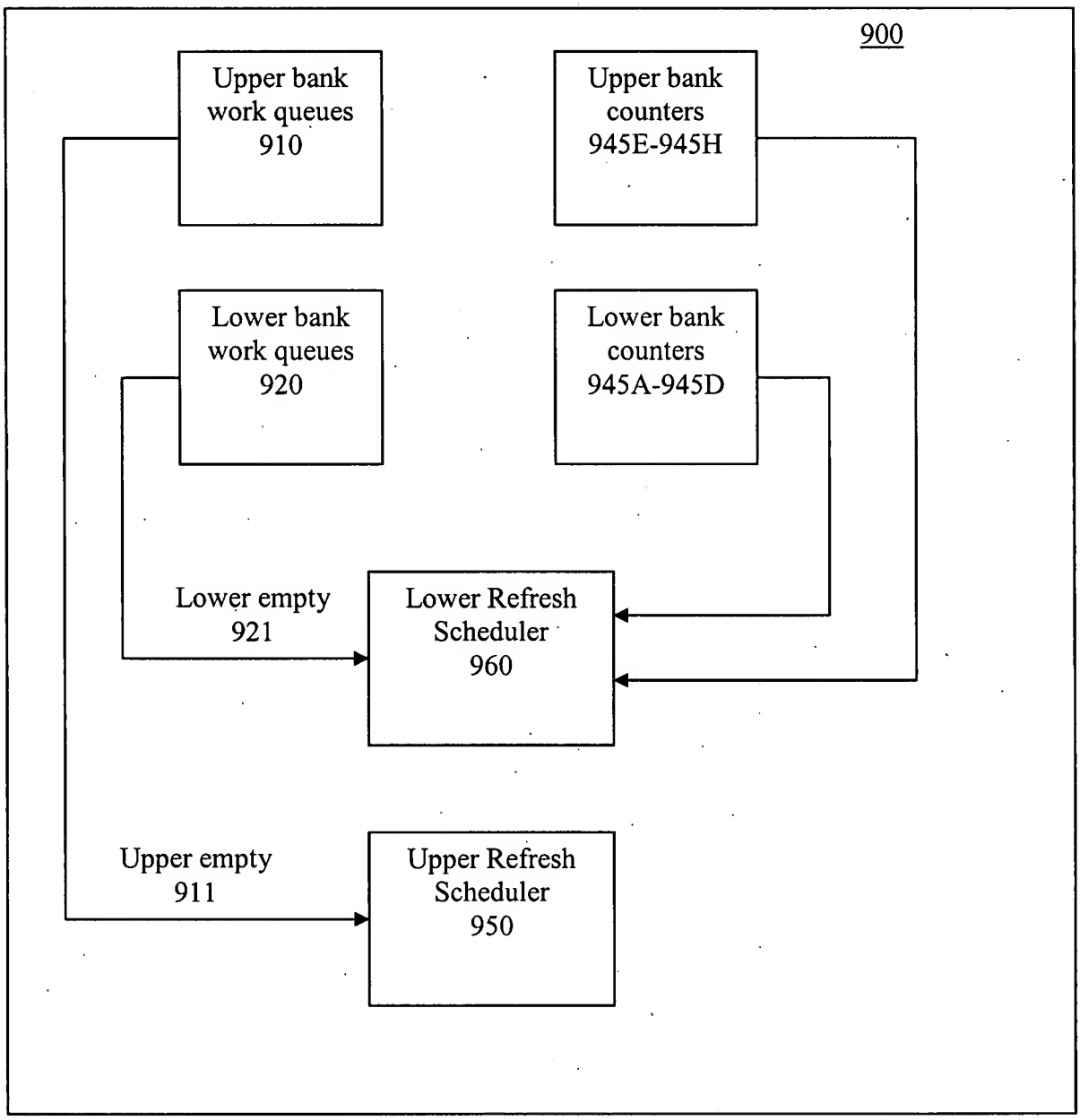
900
Upper bank work queues 910
Upper bank counters 945E-945H
Lower bank work queues 920
Lower bank counters 945A-945D
Lower empty 921
Lower Refresh Scheduler 960
Upper empty 911
Upper Refresh Scheduler 950

FIG. 9

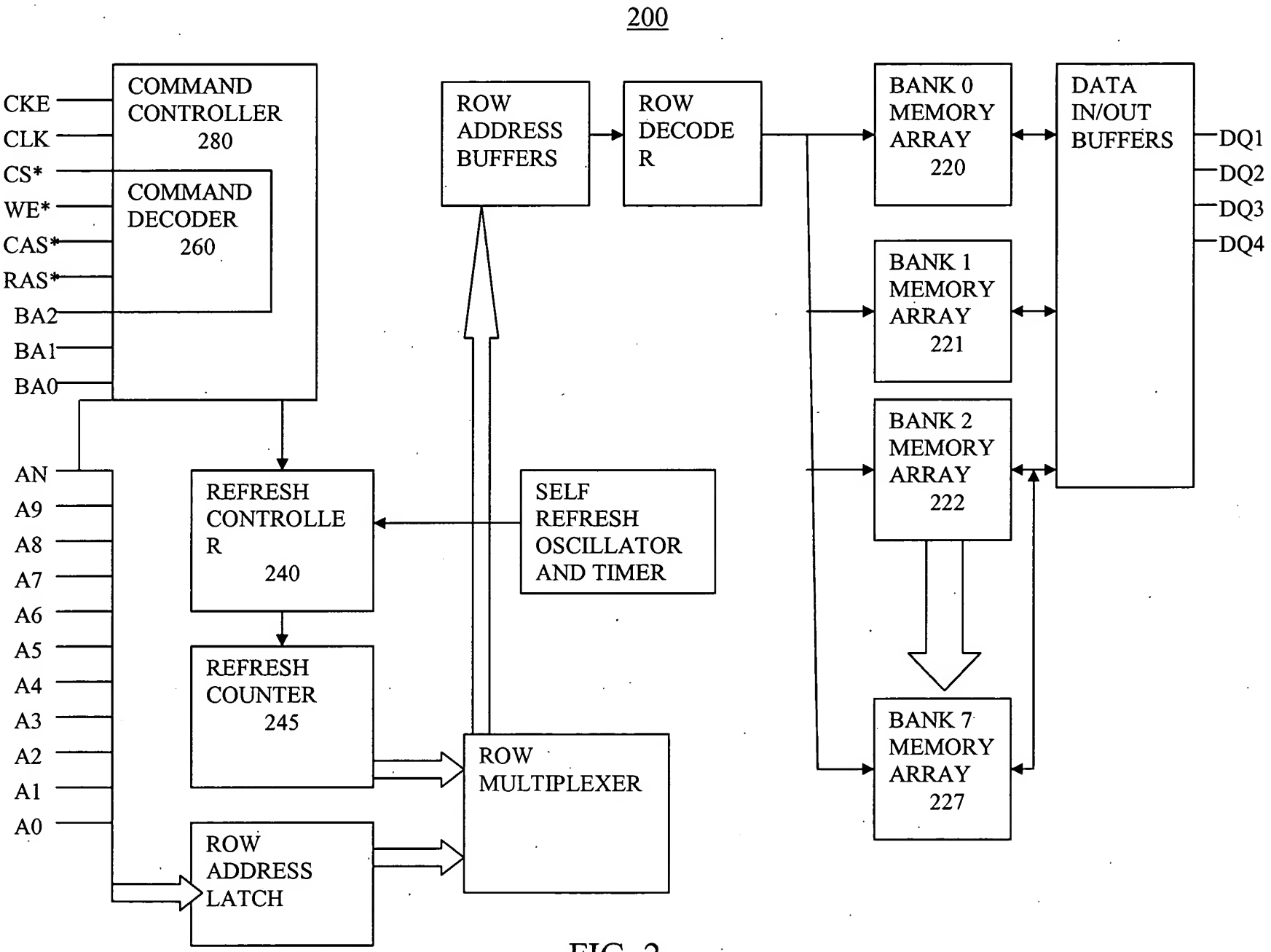
200
CKE
CLK
CS*
WE*
CAS*
RAS*
BA2
BA1
BA0
COMMAND CONTROLLER 280
COMMAND DECODER 260
AN
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
REFRESH CONTROLLER 240
REFRESH COUNTER 245
ROW ADDRESS LATCH
SELF REFRESH OSCILLATOR AND TIMER
ROW ADDRESS BUFFERS
ROW DECODER
ROW MULTIPLEXER
BANK 0 MEMORY ARRAY 220
BANK 1 MEMORY ARRAY 221
BANK 2 MEMORY ARRAY 222
BANK 7 MEMORY ARRAY 227
DATA IN/OUT BUFFERS
DQ1
DQ2
DQ3
DQ4

FIG. 2

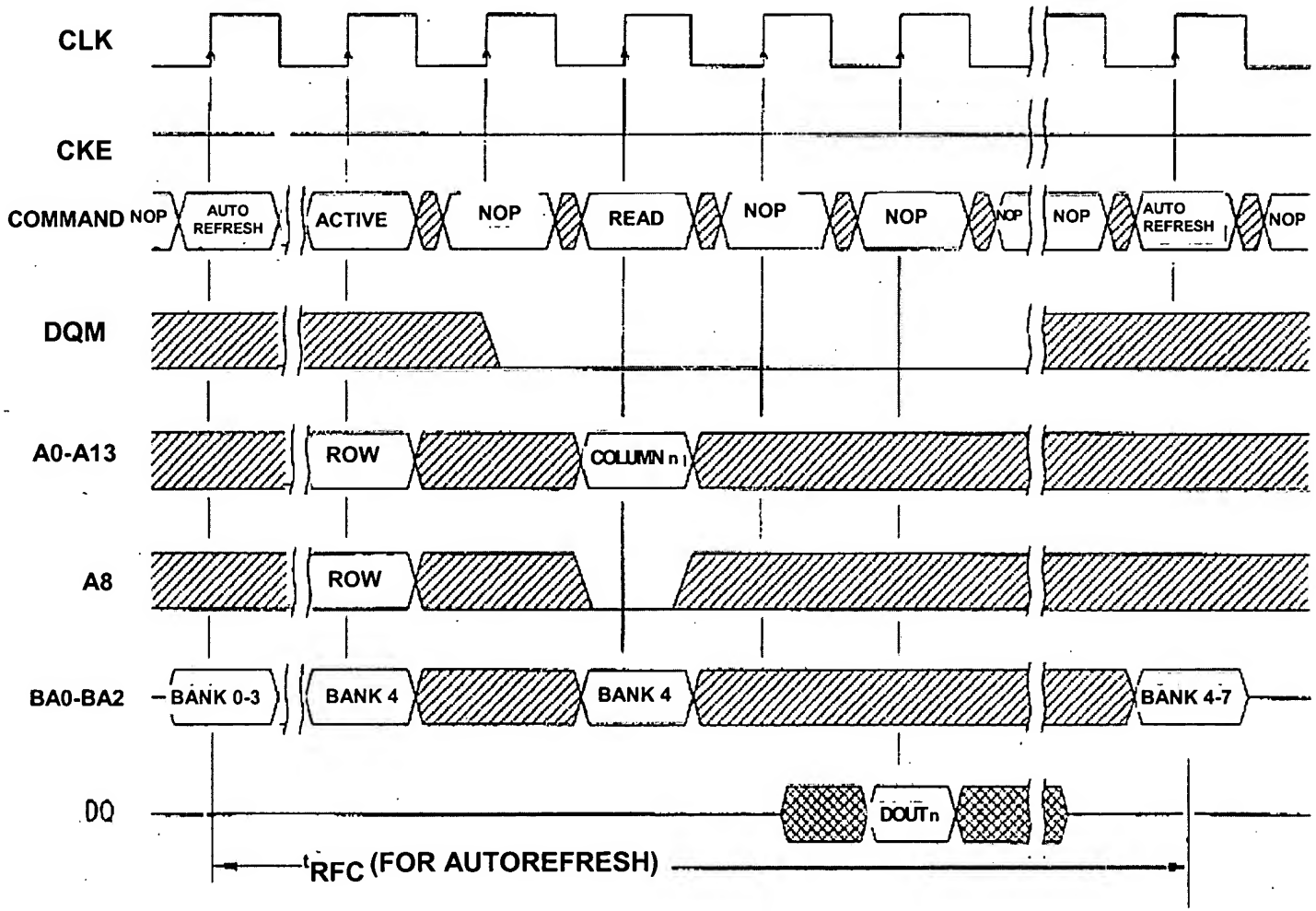

FIG. 3

DON'T CARE

UNDEFINED

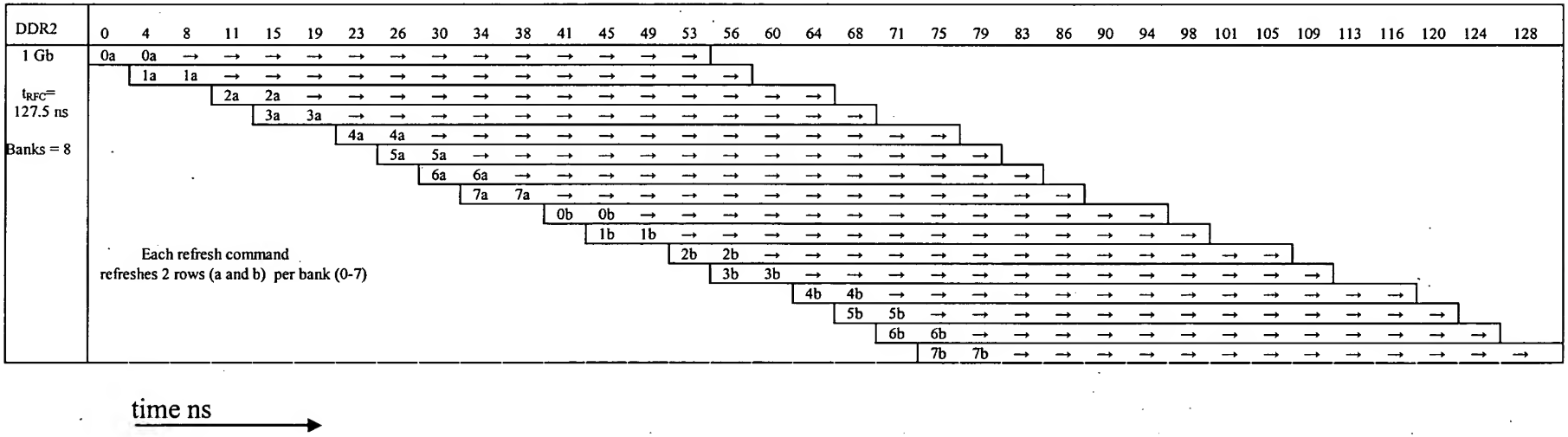
DDR2
1 Gb
t_{RFC}= 127.5 ns
Banks = 8
0 4 8 11 15 19 23 26 30 34 38 41 45 49 53 56 60 64 68 71 75 79 83 86 90 94 98 101 105 109 113 116 120 124 128
0a 0a
1a 1a
2a 2a
3a 3a
4a 4a
5a 5a
6a 6a
7a 7a
0b 0b
1b 1b
2b 2b
3b 3b
4b 4b
5b 5b
6b 6b
7b 7b
Each refresh command refreshes 2 rows (a and b) per bank (0-7)
time ns

FIG. 5

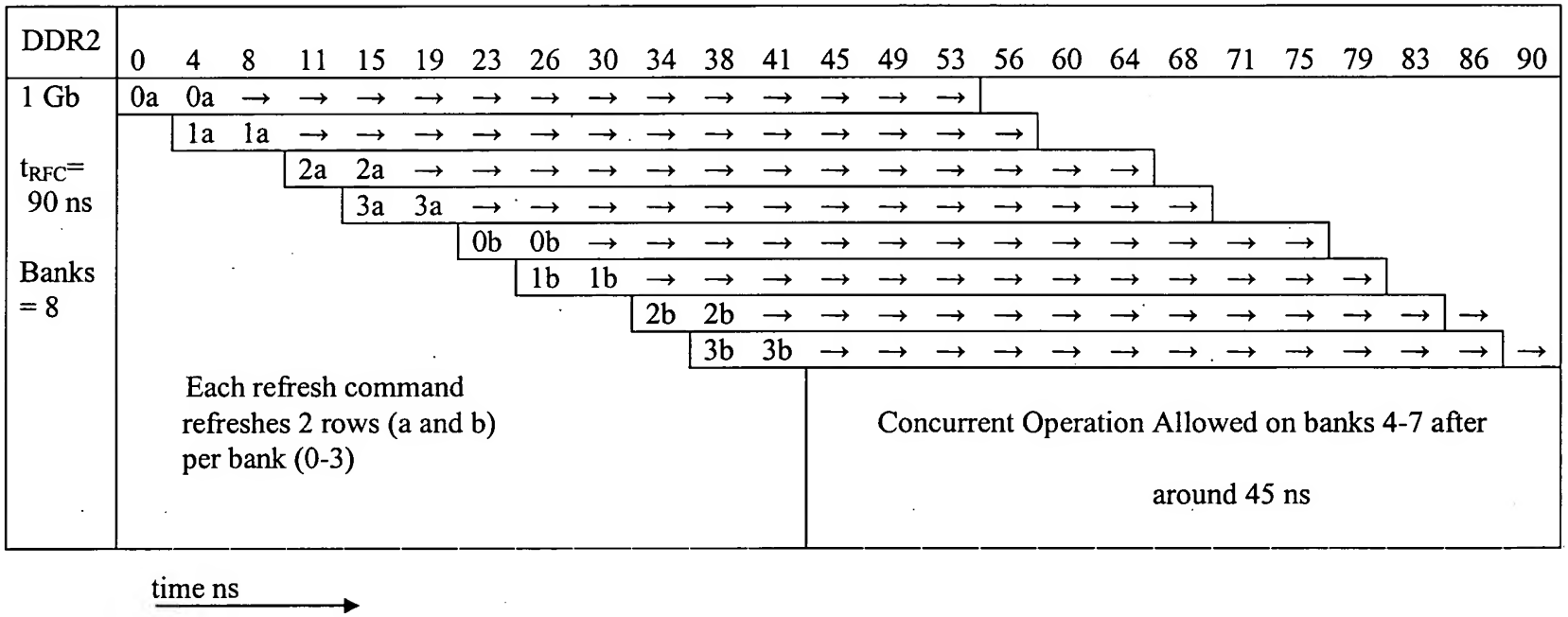
DDR2
1 Gb
t_{RFC}= 90 ns
Banks = 8
0 4 8 11 15 19 23 26 30 34 38 41 45 49 53 56 60 64 68 71 75 79 83 86 90
0a 0a
1a 1a
2a 2a
3a 3a
0b 0b
1b 1b
2b 2b
3b 3b
Each refresh command refreshes 2 rows (a and b) per bank (0-3)
Concurrent Operation Allowed on banks 4-7 after around 45 ns
time ns

FIG. 6

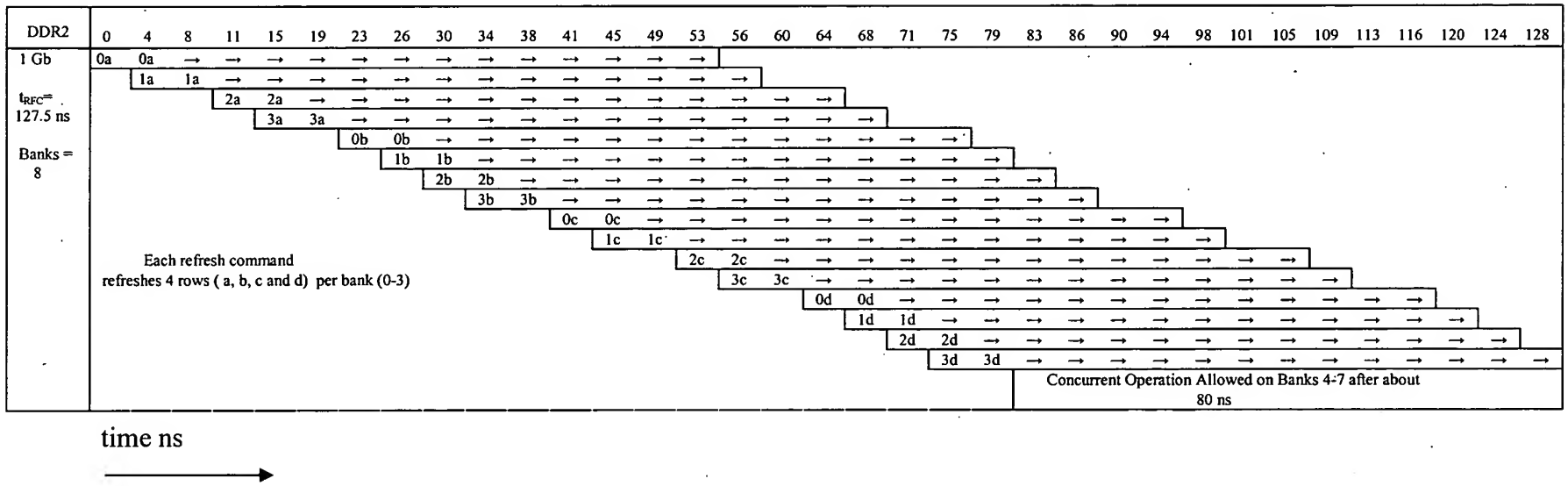
DDR2
1 Gb
t_{RFC}= 127.5 ns
Banks = 8
0 4 8 11 15 19 23 26 30 34 38 41 45 49 53 56 60 64 68 71 75 79 83 86 90 94 98 101 105 109 113 116 120 124 128
0a 0a
1a 1a
2a 2a
3a 3a
0b 0b
1b 1b
2b 2b
3b 3b
0c 0c
1c 1c
2c 2c
3c 3c
0d 0d
1d 1d
2d 2d
3d 3d
Each refresh command refreshes 4 rows (a, b, c and d) per bank (0-3)
Concurrent Operation Allowed on Banks 4-7 after about 80 ns
time ns

FIG. 7

OIPE IAP70 OCT 29 2007 PATENT & TRADEMARK OFFICE

FOR UTILITY/DESIGN
CIP/PCT NATIONAL/PLANT
ORIGINAL/SUBSTITUTE/SUPPLEMENTAL
DECLARATIONS

RULE 63 (37 C.F.R.)
DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PW FORM

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the **INVENTION ENTITLED**

PARTIAL BANK DRAM REFRESH

the specification of which (CHECK applicable BOX(ES))

X A. ☒ is attached hereto.

BOX(ES) → B. ☐ was filed on _____ as U.S. Application No. _____/_____

→ → C. ☐ was filed as PCT International Application No. PCT/ _____/_____ on _____

and (if applicable to U.S. or PCT application) was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56. Except as noted below, I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International Application which designated at least one other country than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International Application, filed by me or my assignee disclosing the subject matter claimed in this application and having a filing date (1) before that of the application on which priority is claimed, or (2) if no priority claimed, before the filing date of this application:

PRIOR FOREIGN APPLICATION(S) Number	Country	Day/MONTH/Year Filed	Date first Laid-open or Published	Date Patented or Granted	Priority NOT Claimed

If more prior foreign applications, X box *at bottom* and continue on attached page.

Except as noted below, I hereby claim domestic priority benefit under 35 U.S.C. 119(e) or 120 and/or 365(c) of the indicated United States applications listed below and PCT international applications listed above or below and, if this is a continuation-in-part (CIP) application, insofar as the subject matter disclosed and claimed in this application is in addition to that disclosed in such prior applications, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56 which became available between the filing date of each such prior application and the national or PCT international filing date of this application:

PRIOR U.S. PROVISIONAL, NONPROVISIONAL AND/OR PCT APPLICATION(S) Application No. (series code/serial no.)	Day/MONTH/Year Filed	Status pending, abandoned, patented	Priority NOT Claimed

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint Pillsbury Winthrop LLP, Intellectual Property Group, 1600 Tysons Boulevard, McLean, VA 22102, telephone number (703) 905-2000 (to whom all communications are to be directed), and the below-named persons (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent, and I hereby authorize them to delete names/numbers below of persons no longer with their firm and to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct the above Firm and/or a below attorney in writing to the contrary.

G. Lloyd Knight	17698	David A. Jakopin	32995	Sean Fitzgerald	32027	James R. Thein	31710
George M. Sirilla	18221	Robert D. Anderson	33826	Leo V. Novakoski	37198	Peter Lam	44855
Alan K. Aldous	31905	Cynthia Thomas Faatz	39973	Mark Seeley	32299	Gene I. Su	45140
Jeffrey S. Draeger	41000	Charles A. Mirho	41199	Raymond J. Werner	34752	Seth Z. Kalson	40670
David J. Kaplan	41105	Kenneth M. Seddon	43105	Calvin E. Wells	43256	Naomi Obinato	39320
Thomas C. Reynolds	32488	Steven C. Stewart	33555	Evan Finkel	49059	Steven C. Skabrat	36279
Howard A. Skaist	36008	Thomas Raleigh Lane	42781	W. Patrick Bengtsson	32456	Robert G. Winkle	37474
Charles K. Young	39435	Mark G. Paulson	30793	Jack S. Barufka	37087	Robin L. Teskin	35030
Dale S. Lazar	28872	Stephen C. Glazier	31361	Adam R. Hess	41835	Anthony L. Miele	34393
Glenn J. Perry	28458	Paul F. McQuade	31542	William P. Atkins	38821	Robert J. Walters	40862
G. Paul Edgell	24238	Richard H. Zaitlen	27248	Paul L. Sharer	36004	Jeffrey D. Karceski	35914
Roger R. Wise	31204	Joseph R. Bond	36458	Richard C. Calderwood	35468		

(1) **INVENTOR'S SIGNATURE:** Howard A. David **Date:** Nov. 3, 2003

	Howard	S.	DAVID
	First	Middle Initial	Family Name
Residence	Portland	Oregon	USA
	City	State/Foreign Country	Country of Citizenship
Post Office Address	3745 SW 48th Place, Portland, Oregon		
(include Zip Code)	97221		

(2) **INVENTOR'S SIGNATURE:** **Date:**

	First	Middle Initial	Family Name
Residence			
	City	State/Foreign Country	Country of Citizenship
Post Office Address			
(include Zip Code)			

FOR ADDITIONAL INVENTORS, "X" box ☐ and proceed on the attached page to list each additional inventor.

☐ See additional foreign priorities on attached page (incorporated herein by reference).

Atty. Dkt. No. PW294374/P15159

PAT-116 2/00

FOR UTILITY/DESIGN CIP/PCT NATIONAL/PLANT ORIGINAL/SUBSTITUTE/SUPPLEMENTAL DECLARATIONS

RULE 63 (37 C.F.R. 1.63) DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PW FORM

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the **INVENTION ENTITLED** **PARTIAL BANK DRAM REFRESH**

the specification of which (CHECK applicable BOX(ES))

X A. ☒ is attached hereto.

BOX(ES) → B. ☐ was filed on _____ as U.S. Application No. _____ / _____

→ → C. ☐ was filed as PCT International Application No. PCT/ _____ / _____ on _____

and (if applicable to U.S. or PCT application) was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56. Except as noted below, I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International Application which designated at least one other country than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International Application, filed by me or my assignee disclosing the subject matter claimed in this application and having a filing date (1) before that of the application on which priority is claimed, or (2) if no priority claimed, before the filing date of this application:

PRIOR FOREIGN APPLICATION(S) Number	Country	Day/MONTH/Year Filed	Date first Laid-open or Published	Date Patented or Granted	Priority NOT Claimed

If more prior foreign applications, X box *at bottom* and continue on attached page.

Except as noted below, I hereby claim domestic priority benefit under 35 U.S.C. 119(e) or 120 and/or 365(c) of the indicated United States applications listed below and PCT international applications listed above or below and, if this is a continuation-in-part (CIP) application, insofar as the subject matter disclosed and claimed in this application is in addition to that disclosed in such prior applications, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56 which became available between the filing date of each such prior application and the national or PCT international filing date of this application:

PRIOR U.S. PROVISIONAL, NONPROVISIONAL AND/OR PCT APPLICATION(S) Application No. (series code/serial no.)	Day/MONTH/Year Filed	Status pending, abandoned, patented	Priority NOT Claimed

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint Pillsbury Winthrop LLP, Intellectual Property Group, 1600 Tysons Boulevard, McLean, VA 22102, telephone number (703) 905-2000 (to whom all communications are to be directed), and the below-named persons (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent, and I hereby authorize them to delete names/numbers below of persons no longer with their firm and to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct the above Firm and/or a below attorney in writing to the contrary.

G. Lloyd Knight	17698	David A. Jakopin	32995	Sean Fitzgerald	32027	James R. Thein	31710
George M. Sirilla	18221	Robert D. Anderson	33826	Leo V. Novakoski	37198	Peter Lam	44855
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Howard A. Skaist	36008	Thomas Raleigh Lane	42781	W. Patrick Bengtsson	32456	Robert G. Winkle	37474
Charles K. Young	39435	Mark G. Paulson	30793	Jack S. Barufka	37087	Robin L. Teskin	35030
Dale S. Lazar	28872	Stephen C. Glazier	31361	Adam R. Hess	41835	Anthony L. Miele	34393
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G. Paul Edgell	24238	Richard H. Zaitlen	27248	Paul L. Sharer	36004	Jeffrey D. Karceski	35914
Roger R. Wise	31204	Joseph R. Bond	36458	Richard C. Calderwood	35468		

(1) INVENTOR'S SIGNATURE: **Date:**

	Howard	S.	DAVID
	First	Middle Initial	Family Name
Residence	Portland	Oregon	USA
	City	State/Foreign Country	Country of Citizenship
Post Office Address	3745 SW 48th Place, Portland, Oregon		
(include Zip Code)	97221		

(2) INVENTOR'S SIGNATURE: **Date:**

	First	Middle Initial	Family Name
Residence			
	City	State/Foreign Country	Country of Citizenship
Post Office Address			
(include Zip Code)			

FOR ADDITIONAL INVENTORS, "X" box ☐ and proceed on the attached page to list each additional inventor.

☐ See additional foreign priorities on attached page (incorporated herein by reference).

Atty. Dkt. No. PW294374/P15159

PAT-116 2/00

Rule 56(a) & (b) = 37 C.F.R. 1.56(a) & (b)
PATENT AND TRADEMARK CASES - RULES OF PRACTICE
DUTY OF DISCLOSURE

(a) ...Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the [Patent and Trademark] Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability...(b) information is material to patentability when it is not cumulative and (1) It also establishes by itself, or in combination with other information, a prima facie case of unpatentability of a claim or (2) refutes, or is inconsistent with, a position the applicant takes in: (i) Opposing an argument of unpatentability relied on by the Office, or (ii) Asserting an argument of patentability

PATENT LAWS 35 U.S.C.

§102. Conditions for patentability; novelty and loss of right to patent

A person shall be entitled to a patent unless--

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent or

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States, or

(c) he has abandoned the invention, or

(d) the invention was first patented or caused to be patented, or was the subject of an inventor's certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor's certificate filed more than twelve months* before the filing of the application in the United States, or

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent, or

(f) he did not himself invent the subject matter sought to be patented, or

(g) before the applicant's invention thereof the invention was made in this country by another who had not abandoned, suppressed, or concealed it. In determining priority of invention there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

§103. Condition for patentability; non-obvious subject matter

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made. . . .

(c) Subject matter developed by another person, which qualified as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

* Six months for Design Applications (35 U.S.C. 172).

Please return signed/recorded to:
Pillsbury Winthrop LLP
Intellectual Property Group
725 South Figueroa Avenue, Suite 2800
Los Angeles, CA 90017-5406

Atty. Dkt. No. PW294374 (Attorney Ref.) | P15159 (Client Ref.)

ASSIGNMENT
OF U.S. ORIGIN PATENT APPLICATION
(to Corporation)
(or Limited Partnership)

WHEREAS, the undersigned, to wit:

Howard S. DAVID

(hereinafter ASSIGNOR), have made an invention known as Dkt. PW 294374

and entitled: **Partial Bank DRAM Refresh**

for which an application for Letters Patent of the United States

☒ was executed even date herewith and is about to be filed in the United States Patent and Trademark Office;

☐ was filed on _____, Appln. No. ____/_____;

AND WHEREAS **Intel Corporation** (hereinafter ASSIGNEE), a corporation duly organized and existing under the laws of the State of **Delaware** and having its principal office and place of business at 2200 Mission College Boulevard, Santa Clara, CA 95054, desires to acquire an interest therein;

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the said ASSIGNOR, does hereby sell, assign and transfer unto ASSIGNEE, its successors, assigns and legal representatives, the entire right, title, and interest for the United States and all foreign countries, in and to any and all improvements that are disclosed in the application for the United States patent that has been executed by the undersigned prior hereto or concurrently herewith on the dates indicated below and is entitled **Partial Bank DRAM Refresh** and in and to said application and all divisional applications, continuation applications, continued prosecution applications, continuation-in-part applications, substitute applications, renewal applications, reissue applications, reexaminations, extensions, and all other patent applications that have been or shall be filed in the United States and all foreign countries on any of said improvements; and in and to all original patents, reissued patents, reexamination certificates, and extensions, that have been or shall be issued in the United States and all foreign countries on said improvements; and in and to all rights of priority resulting from the filing of said United States application;

agree that said ASSIGNEE may apply for and receive a patent or patents for said improvements in its own name; and that, when requested, without charge to, but at the expense of, said ASSIGNEE, its successors, assigns, and legal representatives, to carry out in good faith the intent and purpose of this Assignment, the undersigned will execute all divisional applications, continuation applications, continued prosecution applications, continuation-in-part applications, substitute applications, renewal applications, reissue applications, reexaminations, extensions and all other patent applications on any and all said improvements; execute all rightful oaths, assignments, powers of attorney, and other papers; communicate to said ASSIGNEE, its successors, assigns, and representatives all facts known to the undersigned relating to said improvements and the history thereof; and generally assist said ASSIGNEE, its successors, assigns, or representatives in securing and maintaining proper patent protection for said improvements and for vesting title to said improvements, and all applications for patents and all patents on said improvements, in said

ASSIGNEE, its successors, assigns, and legal representatives; and

covenant with said ASSIGNEE, its successors, assigns, and legal representatives that no assignment, grant, mortgage, license, or other agreement affecting the rights and property herein conveyed has been made to others by the undersigned, and that full right to convey the same as herein expressed is possessed by the undersigned.

NOTE: The undersigned hereby authorizes **PILLSBURY WINTHROP LLP** of the above address to insert hereon any further identification necessary or desirable for recordation of this document.

Executed on the date(s) below indicated.

Each Inventor: Please Sign and Date Below:

_____, 20_____ _____
Date Name: **Howard S. David**

Inventor: Please also list the date that you signed the accompanying DECLARATION AND POWER OF ATTORNEY:

_____, 20_____
Date

725 SOUTH FIGUEROA STREET SUITE 2800 LOS ANGELES, CA 90017-5406 213.488.7100 F: 213.629.1033

October 23, 2003

Stuart B. Chinn
213.488.7205
schinn@pillsburywinthrop.com

PRIVILEGED & CONFIDENTIAL
ATTORNEY-CLIENT COMMUNICATION
ATTORNEY-CLIENT PRIVILEGE
VIA FEDERAL EXPRESS

Howard David
3745 SW 48th Place
Portland, Oregon 97221

Re: Preparation of U.S. Patent Application for:
PARTIAL BANK DRAM REFRESH

Intel Matter No.:	P-15159
Disclosure No.:	24441
Our Ref. No.:	81674-294374

Mr. David:

Please find enclosed a draft of the above-identified patent application that we have been preparing for Intel Corporation. Formal drawing figures are also enclosed herewith.

We understand that you are the inventor, so you must review the application. If there are other inventors, those inventors must also review the application. Please remember that the inventors are the people who, in whole or in part, conceived of the *claimed* subject matter such that one of ordinary skill in the field could build the claimed device or implement the claimed method. In that connection, when you review the claims, make sure that you are the inventors of the subject matter recited therein.

It is our understanding that this invention has not been offered for sale, has not been publicly known or used, and has not been disclosed in a publication *more than one year ago*.. In the United States, any patent application MUST be filed no later than one year after the invention is first offered for sale in the United States, described in a printed publication anywhere in the world, or publicly known or used in the United States. Please let us know immediately if our understanding of the facts is incorrect.
As you review the application, please bear in mind that it is important to consider alternative embodiments of the invention. The alternative embodiments may include the

different ways in which you contemplate implementing or using the invention. If you contemplate additional implementations or uses of the invention, you may want us to describe them in additional figures and corresponding text. We may then add more claims in the application which are directed to these alternative embodiments.

To be complete, the application must teach one of ordinary skill in the art how to make and use the invention in the best mode now known to the inventors. To meet this requirement, it is important that the application contain any information known to you needed to make the claimed subject matter work where that information is not generally known to those of typical skill working in this field. In addition, you should appreciate that if there is any information that is known that makes the device work better in the opinion of the inventor, that information must also be disclosed in the application — regardless, of whether others in the field know this information.

Each claim at the end of the application is a separate definition of the invention. Hence, each claim will afford a different scope of protection. Some claims are more specific than others. We have sought to cover the invention in its broad aspects and in its narrower aspects by drafting many claims.

The claims, which are perhaps the most important part of the application, are the most difficult part of the application to understand. The claims actually define the patent protection that will be asserted. They should be studied carefully. We suggest that you diagram the claims to ensure your full understanding of the claims.

Please note that many of the claims are dependent. Dependent claims refer to other claims by those previous claims' numbers. By doing so, they incorporate by reference the contents of the claims to which they refer. For example, if claim two references claim one, claim two incorporates the entire subject matter of claim one. Further, if claim three refers to claim two, claim three incorporates the subject matter of both claims one and two. As you review the application, please do not hesitate to contact us. Also, if anything needs to be changed, please feel free to make those changes.

Remember that all inventors and anyone else involved in the preparation and prosecution of the application have a *special duty of candor* to the Patent Office. Federal statutes and regulations require you to disclose to the Patent Office any information that is "material" to the examination of the application. Information is material where a substantial likelihood exists that a reasonable Patent Examiner would consider that the information is important in deciding whether to issue a patent. Information relating to public use

(including displays), offers for sale, or published descriptions more than one year ago of the invention or devices related to the invention may well be material.

Also, any prior work by you or others, including publications, devices sold by others, etc. that occurred before you developed your invention may be material. If you are aware of any additional information that may be material, please provide us with such information. Please note that it is better to err on the side of disclosing too much information than to disclose too little information and that this duty continues throughout the prosecution of this patent application.

Attached is the necessary Declaration and Power of Attorney document for you to sign. The Patent Laws require that any individual who signs this Declaration represent that: (1) the contents of the specification (including the claims) have been reviewed and understood; (2) the individual believes himself or herself to be an original and first inventor of the claimed invention; and (3) the individual understands that he or she and all individuals having substantial involvement in the preparation or prosecution of the application have a duty to disclose to the Patent Office information that they are aware of which is *material* to the examination of the application. Failure to comply with the duty of disclosure may well invalidate any subsequent patent. Finally, enclosed is an Assignment document to be signed by all of you as well.

Please take an opportunity to review the draft application and contact us as to any questions or comments that you may have. Please do not hesitate to add or change anything in the patent application. Once you are all satisfied with the application, please execute the formal papers and return them to us for filing as soon as possible.

If you should have any questions, please feel free to contact us. Thank you for your assistance. We look forward to hearing from you soon.

Sincerely,

PILLSBURY WINTHROP LLP

Stuart B. Chinn, Esq.

Enclosures

cc: Roger R. Wise, Esq. (w/o enclosures)